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Grid-Connected Bidirectional Off-Board Electric Vehicle Fast-Charging System

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Abstract

The widespread adoption of electric vehicles (EVs) is contingent on high-power fast-charging infrastructure that can also provide grid stabilization services through bidirectional power flow. While the constituent power stages of such off-board chargers are well-known, a critical research gap exists in their system-level integration, where sub-optimal dynamic interaction between independently controlled stages often leads to DC-link instability and poor transient performance. This paper presents a rigorous, system-level study to address this gap by developing and optimizing a unified control framework for a high-power bidirectional EV fast-charging system. The system integrates a three-phase active front-end rectifier with an LCL filter and a four-phase interleaved bidirectional DC/DC converter. The methodology involves a holistic dynamic modeling of the coupled system, the design of a hierarchical control strategy augmented with a battery current feedforward scheme, and the system-wide optimization of all Proportional–Integral (PI) controller gains using the Artificial Bee Colony (ABC) algorithm. Comprehensive simulation results demonstrate that the proposed optimized control framework achieves a critically damped response, significantly outperforming a conventionally tuned baseline. Specifically, it reduces the DC-link voltage settling time during charging-to-discharging transitions by 74% (from 920 ms to 238 ms) and eliminates voltage undershoot, while maintaining excellent steady-state performance with grid current total harmonic distortion below 1.2%. The study concludes that system-wide metaheuristic optimization, rather than isolated component-level design, is key to unlocking the robust, high-performance operation required for next-generation EV fast-charging infrastructure, providing a validated blueprint for future industrial development.

Keywords: electric vehicles (EV); active rectifier; bidirectional charger; off-board charger; Artificial Bee Colony (ABC); DC-link stability; multiple phases interleave buck–boost DC-DC converter

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1. Introduction

The global push for sustainable energy is fundamentally reshaping the transportation and power sectors, with innovative solutions emerging on two key fronts: hydrogen fuel cell vehicles (HFCVs) for long-range and heavy-duty applications [1,2], and battery electric vehicles (EVs). This transition toward EVs, in particular, stands as a pivotal strategy for mitigating climate change and diminishing reliance on fossil fuels [3–5]. Beyond their role

in decarbonizing transportation, EVs are increasingly valued as versatile grid assets, facilitating the integration of renewable energy sources and enabling ancillary services through bidirectional power flows [6,7]. Nevertheless, the broader adoption of EVs continues to face significant hurdles, chief among them consumer range anxiety, which stems primarily from the inadequate deployment of high-power fast-charging infrastructure [8].

The core technology to address both range anxiety and enable grid services is bidirectional charging, which allows EVs to draw energy from the grid during charging and to inject energy back during discharging [7]. The user convenience of high-power charging comes at a cost, as its high-power demand can introduce significant grid disturbances, including voltage deviations and harmonic distortion [9–11]. Similarly, realizing the potential of discharging requires overcoming parallel challenges to ensure power quality [12]. In both cases, the severity of these issues is directly influenced by the charging system architecture, underscoring its critical importance. A key limitation arises with on-board chargers (OBCs), which are integrated into the vehicle and are typically constrained to powers below 22 kW due to weight, volume, and thermal management concerns [13]. Consequently, for the high-power levels necessary for effective grid services and fast charging, off-board chargers are essential. These systems externalize the power conversion circuitry, as illustrated in Figure 1. This architecture not only supports Level 3 DC fast charging (50–350 kW) but also accommodates the advanced cooling and filtering techniques required for robust bidirectional operation, making it the cornerstone of practical implementation for grid support [14].

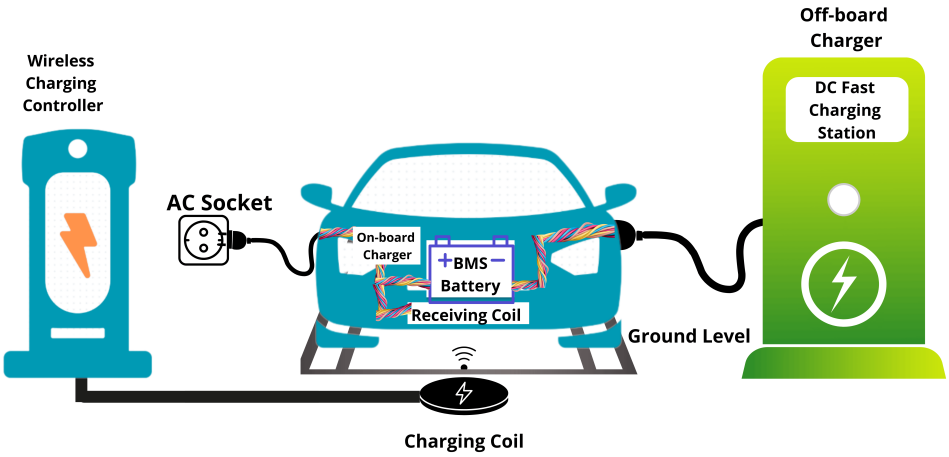

Figure 1. Representative off-board charging architecture supporting bidirectional energy transfer.

Significant research has focused on optimizing the individual components of such off-board systems. However, as synthesized in Table 1, these advancements often remain at the component level, leaving critical system-wide gaps. These gaps can be categorized into three primary limitations that this work aims to address. First, there is a notable absence of co-designed power stage integration. Existing studies often optimize the AC/DC and DC/DC converters independently, overlooking critical interdependencies that compromise the stability of the intermediate DC-link voltage during rapid transitions between charging and discharging modes [15]. Second, and most fundamentally, there is a dearth of unified control frameworks capable of maintaining high performance across the entire operating envelope under realistic, non-ideal grid conditions [16]. Third, control strategies lack dynamic robustness. For example, Proportional–Integral (PI) controllers used in the literature are often tuned using trial-and-error or basic analytical methods. When tuned this way, they exhibit sluggish responses to the abrupt transients inherent in fast-charging applications [17].

Table 1. Critical Analysis of the State-of-the-Art in Bidirectional EV Charging Systems.

Research Focus	Key Advancements	Persistent Limitations
Power Topologies	Soft-switching converters [15], interleaved DC-DC designs [18], active front-end rectifiers [19], and advanced bidirectional DC-DC converters (e.g.,common-ground quadratic SEPIC [20] and coupled-inductor two-phase buck [21])	Isolated component optimization; lack of co-design leading to DC-link stability issues during power flow transitions; limited exploration of system-level integration for novel high-gain topologies.
Grid Interface	LCL filter designs [16,22], harmonic mitigation techniques [23]	Performance analysis under idealized grid conditions, neglecting real-world transients and imbalances
Control Strategies	Cascaded PI control [17], voltage-oriented control(VOC) [24], synchronous reference frame phase-locked loops(SRF-PLL) [25]	Sluggish transient response; insufficient exploration of advanced, coordinated multi-loop tuning methods
System Integration	Bidirectional power flow capability [14], V2G service provision	Independent subsystem optimization; absence of a unified control framework addressing dynamic cross-stage interactions

To bridge these identified gaps, this paper introduces a holistically designed control framework for a high-power, grid-connected, bidirectional off-board EV fast-charging system. The principal contributions of this work are as follows:

- A complete dynamic model of an integrated system comprising a three-phase AC/DC rectifier with an LCL filter and a four-phase interleaved bidirectional DC/DC converter is presented, explicitly capturing the coupling dynamics through the DC-link.
- A hierarchical control framework is developed and is enhanced with a battery current feedforward scheme to actively mitigate DC-link instability during transients.
- The Artificial Bee Colony (ABC) algorithm is implemented to perform a system-wide optimization of all Proportional–Integral (PI) controller gains, moving beyond sub-optimal independent tuning to achieve a critically damped, high-performance response across both power stages.
- Through detailed simulation studies, a quantitative comparative analysis is provided, demonstrating the performance evolution from a baseline analytical design, to a feedforward-enhanced system, and finally to the fully optimized system, highlighting the significant improvements in transient response and power quality.

By advancing the field through systematic optimization and validation rather than component-level innovation, this work provides a validated blueprint and a set of engineering insights for developing high-performance, robust, and industrially relevant bidirectional EV fast-charging systems. The remainder of this paper is structured as follows: Section 2 details the system configuration and dynamic modeling. Section 3 presents the proposed unified control strategy and the ABC optimization process. Section 4 outlines the systematic design of circuit elements and controller parameters. Section 5 discusses the simulation results and performance evaluation, and Section 7 concludes the paper.

2. System Configuration and Modeling

The proposed bidirectional off-board EV fast-charging system is designed to address the limitations of component-level optimization by employing a holistically designed, dual-stage power converter architecture. This section details the complete system configuration and presents the dynamic models essential for the control design in Section 3. The architecture, as is shown in Figure 2, integrates a grid-side AC/DC converter with a battery-side DC/DC converter, decoupled through a common DC-link. Table 2 provides a comprehensive summary of the key system parameters and variables essential for understanding the subsequent modeling and control analysis.

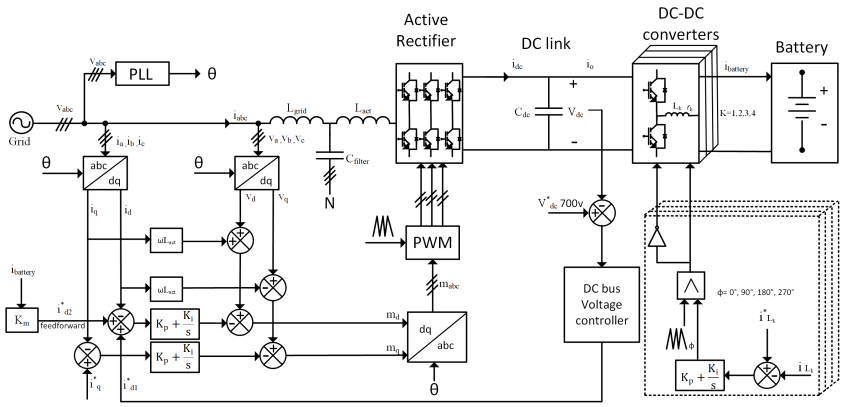

Figure 2. Unified Control Architecture for Grid-Connected Three-Phase Bidirectional Conversion and Multi-Phase Interleaved DC Power Processing.

Table 2. Symbols and Parameters Extracted from Notes.

Symbol	Description	Unit
V_a, V_b, V_c	Grid voltages (Phase-to-neutral voltages)	V
i_a, i_b, i_c	Grid currents	A
i_d, i_q, V_d, V_q	dq-axis components	A, V
V_{LL}	Grid line-to-line voltage	V
E_m	Peak phase voltage	V
$V_{g,1}$	Per-phase RMS voltagee	V
$i_{d1}^*, i_q^*, i_{d2}^*$	Reference current values	A
K_m	Feedforward control gain	–
f_g	Grid frequency	Hz
R_s	Grid source resistance	Ω
L_s	Equivalent grid inductance	H
L_{grid}	Grid-side inductance (LCL filter)	H
L_{act}	Converter-side inductance (LCL filter)	H
C_{filter}	LCL filter capacitor	F
$\omega = 2\pi f_{sw}$	Angular switching frequency	rad/s
f_{sw}	Switching frequency	Hz
i_{dc}	Current output from active rectifier (AR)	A
i_o	Current output of AR after C_{dc}	A
C_{dc}	DC-link capacitor	F
V_{dc}, V_{dc}^*	DC-link voltage (actual, reference)	V
L_k	Phase inductance of Buck–Boost converter	H
r_k	ESR of phase inductance	Ω
$i_{battery}$	Battery current (from IBBC)	A
Φ	Interleaving phase shift	°
i_{Lk}	Current in each phase of Buck–Boost	A
C_{low}	Battery-side capacitor	F

2.1. Overall System Configuration

The complete system topology is illustrated in Figure 3. The configuration is fundamentally dual-stage, comprising a three-phase, grid-connected active front-end rectifier and a four-phase interleaved bidirectional buck–boost DC/DC converter. The AC/DC stage interfaces with the utility grid (415 V line-to-line, 50 Hz) through an LCL filter, which is crucial for attenuating switching harmonics and ensuring compliance with grid codes. This stage is responsible for regulating the DC-link voltage ($V_{dc} = 700$ V) and controlling the power factor. The DC/DC stage interfaces with the EV battery pack (300–450 V) and manages the precise charging/discharging current. The interleaving of four converter phases significantly reduces the current ripple seen by the battery, enhances thermal performance, and improves overall power density. The DC-link capacitor (C_{dc}) acts as an energy buffer between the two stages, decoupling their dynamics and enabling independent control design.

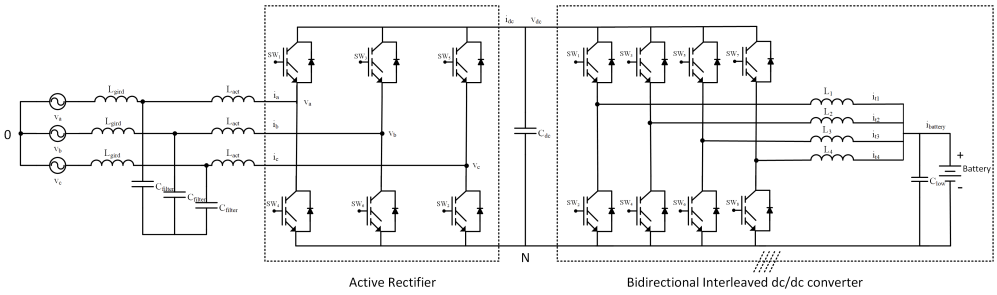

Figure 3. Proposed topology of the bidirectional EV charger system, integrating a three-phase AC/DC active rectifier with an LCL filter and a four-phase interleaved bidirectional DC/DC converter.

The system supports two primary modes of operation:

- **Charging:** where the AC/DC stage operates as an active rectifier to maintain a constant DC-link voltage, while the DC/DC stage operates in buck mode to regulate the battery charging current.
- **Discharging:** where the DC/DC stage operates in boost mode to elevate the battery voltage, and the AC/DC stage operates as an inverter to inject power back into the grid, all while maintaining DC-link voltage stability.

The power semiconductor switches illustrated in Figures 3 and 4 are Insulated Gate Bipolar Transistors (IGBTs). This selection is driven by a holistic evaluation of the system's operational requirements at a DC-link voltage of 700 V and a power level of 50 kW. IGBTs offer a favorable balance of high voltage-blocking capability, robust current handling, and cost-effectiveness in this medium-to-high power range. While wide-bandgap (WBG) devices like SiC MOSFETs offer superior switching performance, recent comparative studies indicate that IGBTs maintain competitive system efficiency at switching frequencies below 25 kHz, as employed here, while providing a significant advantage in terms of component cost and driver maturity [26,27]. Furthermore, the inherent soft-switching characteristics in the interleaved DC-DC stage mitigate the traditional switching loss disadvantage of IGBTs. Their proven ruggedness and excellent safe operating area (SOA) ensure reliable performance during the rapid power flow transitions inherent to bidirectional EV charging, making them a pragmatic and reliable choice for this application [28].

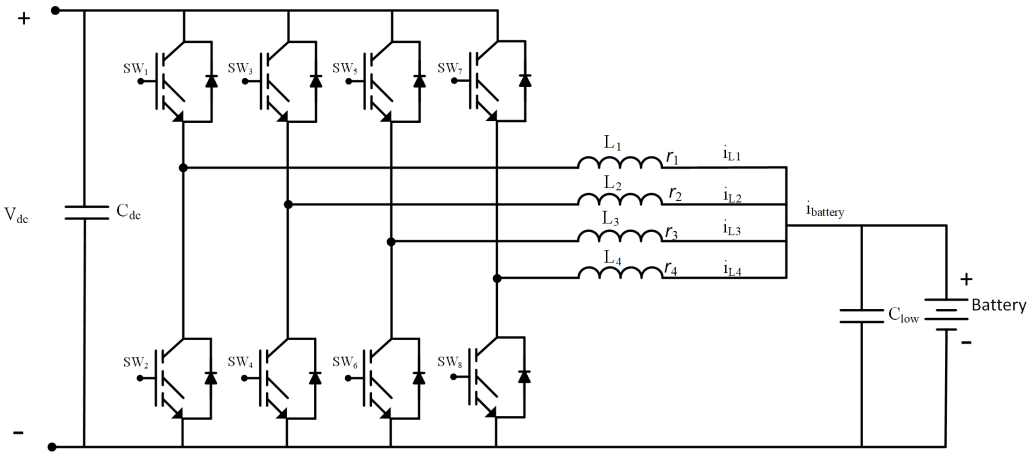

Figure 4. Four-phase interleaved bidirectional buck/boost converter connected to the battery.

2.2. Modeling of the Grid-Connected AC/DC Converter Stage

The grid-interfacing converter represents a critical element within the proposed bidirectional electric vehicle fast-charging system, serving as the primary interface for power exchange between the three-phase AC grid and the internal DC bus. Its performance directly impacts the overall system efficiency, power quality, and stability. A comprehensive dynamic model of this stage, encompassing the voltage source converter (VSC) and its LCL output filter, provides the essential foundation for developing advanced control strategies that ensure unity power factor operation, strict harmonic compliance, and robust DC-link voltage regulation under both charging and discharging operational modes.

The power circuit, as illustrated in Figure 2, employs a standard two-level VSC topology interfaced with the utility grid through an LCL filter. This filter configuration offers superior harmonic attenuation compared to simple L-type filters, thereby enabling reduced switching frequencies while maintaining compliance with grid harmonic standards [22]. For fundamental-frequency modeling and controller synthesis, the LCL network can be approximated by an equivalent series inductance and resistance:

$$L_s = L_{\text{conv}} + L_g, \tag{1}$$

$$R_s = R_{\text{conv}} + R_g, \tag{2}$$

where L_{conv} and L_g are the converter- and grid-side inductances, respectively, and R_{conv}, R_g are their parasitic resistances. This approximation is valid provided that the LCL resonance frequency is placed well above the current-control bandwidth and adequate damping is introduced, ensuring that capacitor dynamics do not affect low-frequency control stability [15,29]. This approximation simplifies the model while preserving accuracy for controller synthesis. In the stationary *abc* frame, the converter and grid dynamics can be described as:

$$v_a = L_s \frac{di_a}{dt} + R_s i_a + v_{aN}, \tag{3}$$

$$v_b = L_s \frac{di_b}{dt} + R_s i_b + v_{bN}, \tag{4}$$

$$v_c = L_s \frac{di_c}{dt} + R_s i_c + v_{cN}, \tag{5}$$

where v_a, v_b, v_c are the grid phase voltages, i_a, i_b, i_c are the grid currents, and v_{aN}, v_{bN}, v_{cN} denote the converter output voltages relative to the converter neutral.

By applying Park's transformation, the dynamics in the synchronous dq reference frame become:

$$v_d = L_s \frac{di_d}{dt} + R_s i_d - \omega L_s i_q + v_{dN}, \tag{6}$$

$$v_q = L_s \frac{di_q}{dt} + R_s i_q + \omega L_s i_d + v_{qN}, \tag{7}$$

where $\omega = 2\pi f_g$ is the grid angular frequency. The terms $\pm\omega L_s i_{q,d}$ represent cross-coupling and must be compensated to obtain decoupled current loops.

The instantaneous active and reactive powers in the synchronous frame are:

$$P = \tfrac{3}{2}\left(v_d i_d + v_q i_q\right), \tag{8}$$

$$Q = \tfrac{3}{2}\left(v_q i_d - v_d i_q\right). \tag{9}$$

with the d-axis aligned to the grid voltage ($v_q \approx 0$), these simplify to:

$$P \approx \tfrac{3}{2} v_d i_d, \tag{10}$$

$$Q \approx -\tfrac{3}{2} v_d i_q, \tag{11}$$

showing that i_d directly controls active power exchange with the grid, while i_q governs reactive power. This property underpins the design of decoupled dq current controllers.

2.3. Modeling of the Interleaved Bidirectional DC–DC Converter

The four-phase interleaved bidirectional DC–DC converter represents a critical component in the proposed electric vehicle fast-charging system, serving as the primary interface between the DC-link and the battery storage system.

As illustrated in Figure 4, this converter topology employs four parallel buck–boost converter phases connected between the DC-link capacitor and battery terminals, with each phase consisting of two active switches with antiparallel diodes, an inductor, and associated filtering components. Each phase $k \in \{1, 2, 3, 4\}$ consists of an inductor L with resistance R_L, two active switches, and complementary gating signals phase-shifted by 90°. This interleaved configuration provides significant advantages in terms of current ripple reduction, improved thermal performance, and enhanced power density compared to conventional single-phase implementations [30,31]. Using the averaged model in continuous conduction mode [32], the inductor dynamics are:

$$L \frac{di_{L_k}}{dt} = d_k v_{dc} - v_{bat} - R_L i_{L_k}, \quad \text{(buck mode)}, \tag{12}$$

$$L \frac{di_{L_k}}{dt} = d_k v_{bat} - v_{dc} - R_L i_{L_k}, \quad \text{(boost mode)}, \tag{13}$$

where $L = L_1 = L_2 = L_3 = L_4$ represents the inductance per phase, $d_k \in [0, 1]$ denotes the duty ratio of phase k, v_{dc} is the DC-link voltage, and v_{bat} is the battery terminal voltage, v_c is the voltage across the output capacitor, and $R_L = r_1 = r_2 = r_3 = r_4$ represents the equivalent series resistance of the inductor. The duty definition is chosen here as the fraction of time the inductor is connected to the instantaneous source in that mode. This approach is particularly suitable for interleaved converters as it captures the essential dynamics while maintaining analytical tractability [33].

The battery-side capacitor dynamics are expressed as:

$$C_{bat} \frac{dv_{bat}}{dt} = \sum_{k=1}^{4} i_{L_k} - i_{bat}, \tag{14}$$

where C_{bat} is the output capacitance, and i_{bat} is the battery current defined as positive when discharging into the converter. The averaged nonlinear state-space model can be formulated in terms of the state vector $\mathbf{x} = [i_{L_1}, i_{L_2}, i_{L_3}, i_{L_4}, v_{bat}]^\top$ and the control vector $\mathbf{u} = [d_1, d_2, d_3, d_4]^\top$ as:

$$\dot{\mathbf{x}} = \mathbf{A}(\mathbf{u})\mathbf{x} + \mathbf{B}(\mathbf{u})v_{dc}. \tag{15}$$

For controller synthesis, small-signal linearization around an operating point yields the per-phase duty-to-current transfer:

$$G_{id}(s) = \frac{\hat{i}_{L_k}(s)}{\hat{d}_k(s)} = \frac{V_{\text{op}}}{Ls + R_L}, \tag{16}$$

where V_{op} is the relevant operating voltage (V_{dc0} in buck mode, V_{bat0} in boost mode), s is the complex frequency variable (Laplace domain), and perturbations are denoted by $\hat{\cdot}$. This simple first-order relation justifies the use of PI controllers for the inductor current loops.

2.4. DC-Link Power Balance and System Coupling

The grid-side and battery-side subsystems are coupled by the common DC-link capacitor. The power balance equation governing its voltage is:

$$\frac{d}{dt}\left(\tfrac{1}{2}C_{dc}V_{dc}^2\right) = P_{ac} - P_{bat}, \tag{17}$$

where P_{ac} is the instantaneous active power exchanged with the grid and P_{bat} is the instantaneous battery power. This can be rewritten as:

$$C_{dc}\frac{dV_{dc}}{dt} = \frac{P_{ac} - P_{bat}}{V_{dc}}. \tag{18}$$

Equation (18) highlights the fundamental coupling between the two stages: the outer DC-link voltage controller regulates V_{dc} by coordinating the i_d current reference of the grid-side converter and the current commands to the DC/DC stage.

2.5. Fundamental Current and Power Relationships

The operational reliability and performance of the proposed converter topology are governed by fundamental current and power relationships that dictate power flow and dynamic interaction between stages. These equations provide the theoretical basis for the control strategy and are essential for validating the circuit's functionality.

The instantaneous power balance at the grid interface is defined by the relationship between AC and DC quantities:

$$p_{ac}(t) = \sum_{k=a,b,c} v_k(t)i_k(t) = v_{dc}(t)i_{dc}(t) + p_{loss,AFE}(t) \tag{19}$$

where i_{dc} is the current injected into the DC-link by the active front-end (AFE) and $p_{loss,AFE}$ accounts for semiconductor losses. Under balanced conditions and with the synchronous reference frame aligned to the grid voltage ($v_q \approx 0$), the steady-state active power transfer simplifies to the well-established relationship:

$$P_{ac} = \frac{3}{2}V_d I_d = V_{dc}I_{dc}. \tag{20}$$

This equation confirms that the grid-side d-axis current I_d directly controls the active power and, consequently, the current I_{dc} supplied to the DC-link, forming the cornerstone of the DC-link voltage regulation loop.

The battery current i_{bat} is the superposition of the currents in the four interleaved phases of the DC/DC converter:

$$i_{bat}(t) = \sum_{k=1}^{4} i_{Lk}(t). \tag{21}$$

The interleaving technique, with a precise 90° phase shift between phases, induces harmonic cancellation. The resulting ripple frequency at the battery terminals is quadrupled relative to the individual phase switching frequency, and the peak-to-peak ripple current is dramatically reduced according to the cancellation factor:

$$CF_{\text{ripple}} = \frac{\Delta i_{bat,pp}}{\Delta i_{Lk,pp}} \approx \frac{1}{N} \cdot \frac{\sin(\pi D/N)}{\sin(\pi D)} \tag{22}$$

where $N = 4$ is the number of phases and D is the duty cycle. This relationship quantitatively predicts the significant ripple reduction that is a key benefit of the chosen topology.

The DC-link capacitor serves as the critical energy buffer, and its current dynamics are paramount for system stability. The current through the capacitor i_{Cdc} is defined by the difference between the grid-side and battery-side currents:

$$i_{Cdc}(t) = C_{dc}\frac{dv_{dc}}{dt} = i_{dc}(t) - i_o(t) \tag{23}$$

where i_o is the current drawn by the DC/DC converter from the DC-link. This equation highlights the fundamental coupling mechanism: system stability requires that the power balance $P_{ac} \approx P_{bat}$ is maintained such that the low-frequency component of i_{Cdc} remains bounded, ensuring stable DC-link voltage v_{dc} during operational transients.

2.6. Efficiency Analysis and Power Loss Calculation

A rigorous efficiency analysis is indispensable for assessing the performance and economic viability of the proposed fast-charging system. The overall system efficiency, η_{sys}, is defined as the ratio of useful output power to total input power. For charging mode (G2V), this represents the power delivered to the battery relative to the power drawn from the grid, with the relationship reversed for discharging (V2G). This is formally expressed as:

$$\eta_{sys} = \frac{P_{output}}{P_{input}} = \frac{P_{output}}{P_{output} + P_{loss,total}} \tag{24}$$

where $P_{loss,total}$ is the aggregate power dissipation. This total loss is the sum of contributions from the grid-side active front-end (AFE) rectifier and the battery-side interleaved bidirectional buck–boost converter (IBBC):

$$P_{loss,total} = P_{loss,AFE} + P_{loss,IBBC}. \tag{25}$$

The loss model for the IBBC must accurately capture its multi-phase, bidirectional operation. The total power loss in this stage, $P_{loss,IBBC}$, aggregates losses from semiconductors and passive components:

$$P_{loss,IBBC} = \sum_{k=1}^{4}(P_{cond,SW_k} + P_{sw,SW_k}) + \sum_{k=1}^{4}(P_{cond,D_k} + P_{sw,D_k}) + P_{loss,L} + P_{loss,C} \tag{26}$$

where the subscripts SW_k and D_k refer to the k-th active switch and its parallel diode, respectively.

Conduction losses arise from the finite on-state resistance of the MOSFETs and the forward voltage drop of the body diodes. For each MOSFET, the conduction loss is calculated from its on-state resistance $R_{DS(on)}$ and the RMS current, $I_{SW_k,rms}$:

$$P_{cond,SW_k} = R_{DS(on)} \cdot I^2_{SW_k,rms}. \tag{27}$$

Similarly, the conduction loss in the diodes depends on their forward voltage V_F and the average current, $I_{D_k,avg}$:

$$P_{cond,D_k} = V_F \cdot I_{D_k,avg}. \tag{28}$$

Switching losses, a critical factor at high frequency, are estimated from the switching energy per transition. The total switching loss for a single switch at frequency f_{sw} is approximated by:

$$P_{sw,SW_k} = f_{sw} \cdot (E_{on} + E_{off}) \approx f_{sw} \cdot \frac{V_{dc} \cdot I_{Lk}}{I_{ref}} \cdot t_{cross} \tag{29}$$

where I_{Lk} is the inductor current in phase k, and t_{cross} is the current-voltage overlap time.

Losses in the passive components are equally significant. Each phase inductor exhibits copper loss due to its equivalent series resistance R_L and core losses. The copper loss for one phase is:

$$P_{loss,L_k} = R_L \cdot I^2_{Lk,rms} \tag{30}$$

with the total inductor loss summed over all phases: $P_{loss,L} = \sum_{k=1}^{4} P_{loss,L_k}$. For the capacitors, losses are primarily due to the Equivalent Series Resistance (ESR), dissipated by the RMS ripple current $I_{C,rms}$:

$$P_{loss,C} = ESR \cdot I^2_{C,rms}. \tag{31}$$

The severe ripple current stress on C_{dc}, derived from the power balance in Equation (18), makes this a particularly significant loss component.

For the three-phase AFE, losses are again dominated by its power semiconductors. Conduction losses for the IGBT/MOSFET switches and their anti-parallel diodes are modeled using the same principles, based on $R_{DS(on)}$ (or $V_{CE(sat)}$) and V_F with their respective current waveforms. Switching losses in the AFE are substantial due to the high DC-link voltage ($V_{dc} = 700\ V$) and are calculated analogously to the DC/DC stage, influenced by grid phase currents. Finally, the LCL filter contributes losses through the parasitic resistances of its inductors, R_g and R_{conv}, as defined in Equations (1) and (2):

$$P_{loss,LCL} = (R_g + R_{conv}) \cdot I^2_{g,rms} \tag{32}$$

where capacitor branch losses are typically negligible.

This holistic loss model, when parameterized with data from Table 2, enables a high-fidelity prediction of the system's efficiency curve across its operating range. Furthermore, it quantitatively justifies the efficiency gains achieved through the interleaving technique, which reduces per-phase currents and thus I^2R losses, and the ABC optimization, which minimizes transient currents and associated switching losses. This analytical approach is aligned with established methodologies for loss calculation in power electronic systems [34].

2.7. Voltage and Current Stress Analysis on Power Switches

A critical aspect of ensuring the reliability and practical viability of the proposed converter topology is the rigorous analysis of electrical stresses on the power semiconductor switches. These stresses dictate component selection, thermal management design, and the overall system's operational robustness. The following analysis, based on established

power electronics principles [33,35], quantifies the worst-case voltage and current stresses for both conversion stages.

The IGBTs in the three-phase VSC must withstand the DC-link voltage including overshoot from switching transients:

$$V_{CE,\max} \approx 1.2 \times V_{dc} = 840 \text{ V}. \tag{33}$$

This necessitates 1200 V-rated devices. The RMS current stress per switch, which governs conduction losses, is calculated for the maximum grid current $I_{g,\max} = 400\ \text{A}_{\text{RMS}}$:

$$I_{C,\text{RMS}} = I_{g,\max} \cdot \sqrt{\frac{1}{8} + \frac{M \cos\phi}{3\pi}} \approx 283 \text{ A}. \tag{34}$$

In boost mode (V2G), the lower switches block the full DC-link voltage ($V_{dc} = 700$ V), while in buck mode (G2V), the upper switches withstand the maximum battery voltage ($V_{bat,\max} = 450$ V). The interleaving architecture reduces the current stress per device. The RMS current per switch is:

$$I_{SW,\text{RMS}} = \frac{I_{bat}}{N} \cdot \sqrt{D} \approx 25 \text{ A}, \tag{35}$$

for a total battery current $I_{bat} = 100$ A distributed over $N = 4$ phases.

3. Control Strategy Design and Optimization

The modeling results derived above directly shape the controller structure. A critical step in this synthesis is the selection of a control paradigm capable of managing the multi-variable, bidirectional nature of the high-power fast-charging system. The design of the control architecture was guided by the core requirement of maintaining robust DC-link stability while coordinating the AC/DC and DC/DC power stages during rapid charge/discharge transitions. New-generation AI-based controllers, such as fuzzy logic and neural networks, excel in handling system nonlinearities and uncertainties without requiring precise models [20,36]. In parallel, state-space approaches, particularly Model Predictive Control (MPC), offer a powerful framework for explicit constraint handling and managing the multi-variable interactions inherent in our system [21,37]. However, the application of these advanced controllers to a tightly coupled, multi-stage system presents significant practical challenges. The computational burden of online MPC is often prohibitive for the high-bandwidth inner-loop current control required here. Similarly, the deployment of many AI-based agents is complicated by sample-time sensitivity and a lack of extensive validation for system-wide coordination, where the dynamics of one stage (e.g., the DC/DC converter) directly impact another (e.g., the DC-link voltage via the AC/DC converter) [38]. Consequently, a cascaded PI control structure was selected as the foundational architecture. Its key advantage lies in its practical implementability and proven reliability. To overcome the inherent limitations of standard PI tuning, we introduce a system-level metaheuristic optimization (Artificial Bee Colony, detailed in Section 5.2) that globally tunes all controller parameters concurrently. This approach effectively embeds a high degree of robustness and coordination into a well-understood and industrially viable control framework, achieving performance competitive with more complex controllers while remaining feasible for immediate deployment.

From the dq-frame equations of the AC/DC converter, it is evident that the d-axis current regulates the active power and DC-link voltage, while the q-axis current governs the reactive power exchange with the grid. The small-signal dynamics of the interleaved DC/DC converter reveal that each inductor current behaves as a first-order system with

duty ratio modulation as the control input. Finally, the DC-link balance equation highlights the supervisory layer that coordinates grid-side current references and battery-side current flow. Together, these control-oriented models provide the exact transfer functions $G_{i,ac}(s)$, $G_{i,bat}(s)$, and $G_v(s)$, which form the basis for the hierarchical control strategy presented in this section.

The overall control framework is organized hierarchically to guarantee stable bidirectional power flow, robust DC-link regulation, and strict compliance with grid standards. Figure 2 illustrates the unified architecture, in which inner current controllers for both the AC/DC and DC/DC stages are embedded within outer voltage regulation loops, supported by a phase-locked loop (PLL) for synchronization and a feedforward mechanism for enhanced transient response.

3.1. Inner Current Control Loops

The first layer of the control hierarchy is the inner current regulation. The modeling in Section 2 showed that both the AC and DC sides reduce to first-order plants, making them well suited for PI control. On the grid side, using the equivalent series inductance and resistance of the LCL filter, the plant dynamics of each axis are expressed as:

$$G_{i,ac}(s) = \frac{I(s)}{V^*(s)} = \frac{1}{L_s s + R_s}. \tag{36}$$

On the battery side, small-signal analysis of the interleaved DC/DC stage yields:

$$G_{i,bat}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{\text{op}}}{Ls + R_L}, \tag{37}$$

Both plants are compensated by PI controllers of the form $C(s) = K_p + K_i/s$. The controller parameters are designed via pole-placement to achieve a desired closed-loop response characterized by a natural frequency ω_n and damping ratio ζ. The closed-loop transfer function for a system with open-loop $L(s) = C(s)G(s)$ has a characteristic equation of $1 + L(s) = 0$. Substituting the plant and controller models yields:

$$1 + \left(K_{p,idc} + \frac{K_{i,idc}}{s}\right)\frac{V_{\text{op}}}{Ls + R} = 0. \tag{38}$$

Multiplying through by $s(Ls + R)$ and rearranging terms gives the characteristic equation:

$$Ls^2 + (R + V_{\text{op}}K_{p,idc})s + V_{\text{op}}K_{i,idc} = 0. \tag{39}$$

This is equated to the desired second-order characteristic equation $s^2 + 2\zeta\omega_n s + \omega_n^2 = 0$. Normalizing Equation (39) by dividing by L allows for coefficient comparison:

$$\frac{R + V_{\text{op}}K_{p,idc}}{L} = 2\zeta\omega_n, \tag{40}$$

$$\frac{V_{\text{op}}K_{i,idc}}{L} = \omega_n^2. \tag{41}$$

Solving for the PI gains provides the final design equations:

$$K_{p,idc} = \frac{2\zeta\omega_n L - R}{V_{\text{op}}}, \tag{42}$$

$$K_{i,idc} = \frac{\omega_n^2 L}{V_{\text{op}}}. \tag{43}$$

These controllers ensure decoupled dq current regulation on the grid side and precise inductor current tracking on the battery side, directly reflecting the models developed earlier.

3.2. Outer DC-Link Voltage Regulation

The supervisory function of the control system is the DC-link voltage regulation. The plant model for this loop is derived from the nonlinear power balance equation, which is linearized around a nominal operating point (V_{dc0}, I_{d0}). Starting from the power balance:

$$\frac{d}{dt}\left(\tfrac{1}{2}C_{dc}V_{dc}^2\right) = P_{ac} - P_{bat}. \tag{44}$$

Assuming the inner current loop forces $i_d \approx i_d^*$ and aligning the dq-frame such that $P_{ac} \approx \frac{3}{2}v_d i_d$, the equation becomes:

$$C_{dc}V_{dc}\frac{dV_{dc}}{dt} = \frac{3}{2}v_d i_d^* - P_{bat}. \tag{45}$$

Applying small-signal perturbation ($V_{dc} = V_{dc0} + \hat{v}_{dc}$, $i_d^* = I_{d0} + \hat{i}_d^*$) and neglecting the product of perturbation terms and the disturbance P_{bat} yields the linearized model:

$$C_{dc}V_{dc0}\frac{d\hat{v}_{dc}}{dt} \approx \frac{3}{2}V_{d0}\hat{i}_d^*. \tag{46}$$

Taking the Laplace transform gives the simplified plant transfer function:

$$G_v(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_d^*(s)} = \frac{K_v}{C_{dc}s}, \qquad \text{where} \quad K_v = \frac{3V_{d0}}{2V_{dc0}}. \tag{47}$$

This pure integrator plant motivates the use of a PI regulator:

$$C_v(s) = K_{p,vdc} + \frac{K_{i,vdc}}{s}, \tag{48}$$

which provides proportional action for response speed and integral action for zero steady-state error. The bandwidth of this outer loop is chosen at least one decade below that of the inner current loops to ensure stable cascaded control.

3.3. Grid Synchronization Using PLL

Accurate grid synchronization is essential to align the dq-frame with the grid voltage vector. The PLL design builds directly on the dq model, where proper alignment ensures that $v_q \approx 0$ and hence i_d and i_q regulate active and reactive power independently. The adopted synchronous reference frame PLL (SRF-PLL) uses a PI controller to regulate the q-component of the grid voltage to zero. The closed-loop transfer function from the actual grid phase θ to the estimated phase $\hat{\theta}$ is given by:

$$G_{\text{PLL}}(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{K_{p,\text{PLL}}s + K_{i,\text{PLL}}}{s^2 + K_{p,\text{PLL}}s + K_{i,\text{PLL}}}, \tag{49}$$

where $K_{p,\text{PLL}}$ and $K_{i,\text{PLL}}$ are the PI gains. These parameters are tuned to achieve adequate phase margin (typically $> 45^\circ$) for fast dynamic response and robust disturbance rejection under unbalanced grid conditions.

3.4. Feedforward Compensation for Transient Enhancement

The DC-link power balance model also motivates the inclusion of feedforward control to improve transient performance. The goal is to compute the d-axis current required to

supply the battery power $P_{bat} \approx V_{dc} i_{bat}$ instantaneously. From the active power balance $P_{ac} = P_{bat}$ and the equation $P_{ac} \approx \frac{3}{2} v_d i_d$, the feedforward current is:

$$i^*_{d,ff} = \frac{2}{3} \frac{P_{bat}}{v_d} \approx \frac{2}{3} \frac{V^*_{dc} i_{bat}}{v_d}, \tag{50}$$

where V^*_{dc} is the DC-link voltage reference. The total d-axis current reference is then:

$$i^*_d = i^*_{d,fb} + i^*_{d,ff} = i^*_{d,fb} + \frac{2}{3} \frac{V^*_{dc} i_{bat}}{v_d}. \tag{51}$$

Using the reference voltage V^*_{dc} instead of the measured V_{dc} avoids introducing an algebraic loop. This term immediately compensates for disturbances caused by battery current variations, reducing the burden on the feedback controller.

3.5. Control of the Interleaved DC-DC Converter

For the interleaved converter, the small-signal control-to-inductor-current transfer function identified in the modeling stage is:

$$G_{id}(s) = \frac{\hat{i}_{L_k}(s)}{\hat{d}_k(s)} = \frac{V_{\text{op}}}{Ls + R_L}, \tag{52}$$

where $V_{\text{op}} = V_{dc}$ in buck mode and $V_{\text{op}} = V_{bat}$ in boost mode. This first-order plant justifies the use of a PI controller for each phase current loop. Using pole-placement tuning for a desired closed-loop bandwidth ω_n and damping ratio ζ, the controller gains are:

$$K_{p,vdc} = \frac{2\zeta\omega_n L - R_L}{V_{\text{op}}}, \tag{53}$$

$$K_{i,vdc} = \frac{\omega_n^2 L}{V_{\text{op}}}. \tag{54}$$

This design ensures accurate bidirectional current regulation. The interleaving of the phase carriers, phase-shifted by 90°, provides the additional benefit of significant ripple cancellation at the battery terminals.

3.6. Optimization of PI Controllers Using ABC Algorithm

Although the analytical tuning described above guarantees stability and satisfactory transient response, it is sensitive to parameter variations and nonlinearities. To address this limitation and achieve superior performance across the entire operating range, the controller gains are refined using the Artificial Bee Colony (ABC) optimization algorithm, a sophisticated metaheuristic technique inspired by honeybee foraging behavior [39]. Each candidate solution encodes the complete set of PI parameters, including those of the current controllers, voltage regulator, and PLL. The optimization is driven by a multi-objective cost function:

$$J = \alpha \int_0^T e^2_{V_{dc}}(t)\, dt + \beta \int_0^T e^2_{\theta}(t)\, dt, \tag{55}$$

where $e_{V_{dc}}$ denotes the DC-link voltage error, e_θ the phase error of the PLL, and α, β weighting coefficients that balance voltage stability and synchronization accuracy. The ABC-based optimization achieves superior performance compared to purely analytical design, leading to faster settling times, reduced overshoot, and enhanced robustness under a wide range of grid and load conditions.

The ABC algorithm implements a population-based optimization strategy that mimics the foraging behavior of honeybee colonies [40]. ABC is particularly advantageous for

engineering optimization tasks due to its simplicity, requiring fewer tunable parameters than alternatives like Genetic Algorithms (GA) and Particle Swarm Optimization (PSO), while exhibiting faster convergence and robust exploration-exploitation balance [41,42]. Recent comparative studies in power electronics underscore these benefits. For instance, ABC optimization yielded superior objective function values (e.g., reduced ITAE by up to 20%) and shorter execution times than PSO, for robust control of interlinking converters in hybrid microgrids [43,44]. The complete optimization procedure follows the systematic flowchart shown in Figure 5, which details the iterative process of solution generation, evaluation, and refinement.

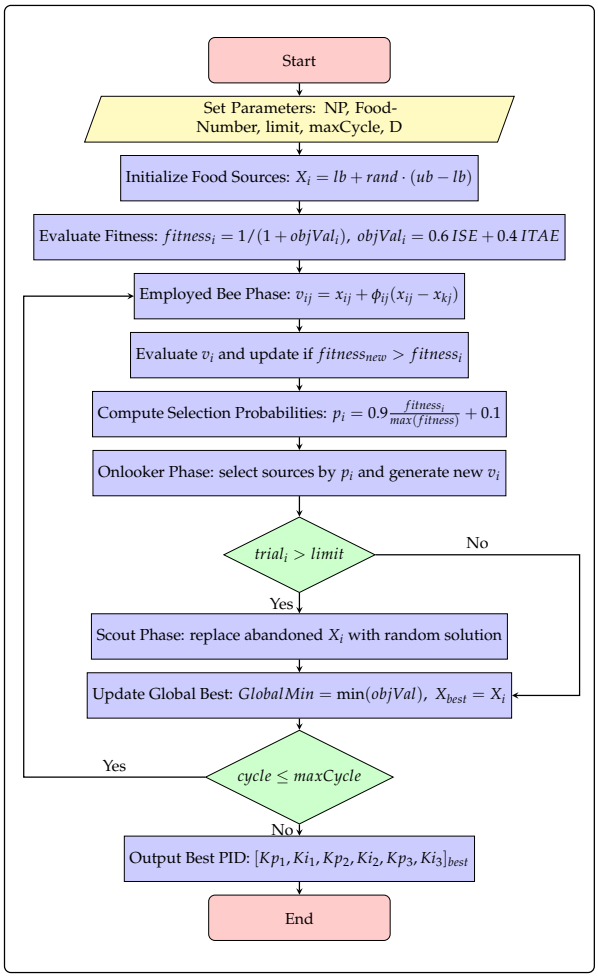

Figure 5. Flowchart of the ABC Algorithm.

The optimization process begins with parameter initialization, where key algorithm parameters such as colony size (NP), food number, abandonment limit, maximum cycles (maxCycle), and problem dimension (D) are defined. The algorithm then proceeds to initialize food sources representing potential solutions using the equation $X_i = lb + rand \cdot (ub - lb)$, where each solution encodes the complete set of PI parameters: $\mathbf{x}_i = [K_{p,idc}, K_{i,idc}, K_{p,vdc}, K_{i,vdc}, K_{p,\mathrm{PLL}}, K_{i,\mathrm{PLL}}]$.

Each candidate solution undergoes fitness evaluation using the objective function $objVal_i = 0.6\,ISE + 0.4\,ITAE$, which combines integral squared error and integral time-weighted absolute error metrics to balance rapid response with long-term stability. The fitness is calculated as $fitness_i = 1/(1 + objVal_i)$, with higher values indicating better solutions.

The employed bee phase conducts local searches around existing solutions using the mutation equation $v_{ij} = x_{ij} + \phi_{ij}(x_{ij} - x_{kj})$, where ϕ_{ij} is a random number in $[-1, 1]$. New

solutions are evaluated and retained if they exhibit improved fitness. The onlooker bee phase then selects promising solutions probabilistically based on selection probabilities $p_i = 0.9\frac{fitness_i}{max(fitness)} + 0.1$, intensifying the search in regions with higher fitness values.

Solutions that fail to improve beyond the abandonment limit ($trial_i > limit$) enter the scout bee phase, where they are replaced with randomly generated solutions to maintain population diversity and prevent premature convergence to local optima. The global best solution is updated after each cycle, and the process iterates until the maximum cycle count is reached. The specific parameters used for the ABC optimization are detailed in Table 3, which were determined through extensive preliminary testing to balance computational efficiency with solution quality.

Table 3. ABC algorithm parameters for PI controller optimization.

Parameter	Value/Range
Colony size (SN)	20–50
Number of parameters (D)	6
Maximum cycles (MCN)	1000
Abandonment limit ($limit$)	$SN \times D$
K_p, K_i search range	[0, 10]
Random number (r)	[0, 1]
Objective function (J)	Weighted ISE + ITAE

4. Systematic Design of Circuit Elements and Controller Parameters

Building upon the control-oriented models and design equations established in Section 3, this section presents a systematic procedure for determining both the passive component values and controller parameters of the proposed bidirectional EV fast-charging system. The design process follows a hierarchical approach, beginning with the analytical computation of controller gains using the derived transfer functions and pole-placement techniques, and concluding with refinement through metaheuristic optimization to enhance robustness and performance.

Table 4 summarizes the complete set of system specifications, passive component values, and controller parameters obtained through this systematic design procedure, including both analytically derived and ABC-optimized values.

4.1. Analytical Controller Design

The controller parameters are systematically derived using the mathematical framework developed in Section 3. For the grid-side current control, the plant dynamics $G_{i,ac}(s) = 1/(L_{act}s + R)$ with $L_{act} = 0.112$ mH and $R = 1.0\ \Omega$ form the basis for PI controller design. Setting the current loop bandwidth to one-tenth of the switching frequency ($f_{sw} = 10$ kHz) yields:

$$\omega_{i,sw} = \frac{2\pi f_{sw}}{10} \approx 6283 \text{ rad/s}. \tag{56}$$

Applying the pole-placement design equations $K_p = (2\zeta\omega_n L - R)/V_{op}$ and $K_i = (\omega_n^2 L)/V_{op}$ with $\zeta = 0.707$ and $V_{op} = 339.4$ V produces the current controller gains:

$$K_{p,idc} = L_{act} \cdot \omega_{i,sw} - R = 0.7027, \tag{57}$$

$$K_{i,idc} = R \cdot \omega_{i,sw} = 6.283. \tag{58}$$

For the DC-link voltage regulation, the plant model $G_v(s) = K_v/(C_{dc}s)$ with $K_v = 3V_{d0}/(2V_{dc0})$ guides the controller design. Using $V_{dc}^* = 700$ V, $C_{dc} = 95.5$ mF, $E_m = 339.4$ V, and a desired response time of $(t_1 - t_0) = 20$ ms, the voltage controller gains are calculated as:

$$K_{p,vdc} = \frac{2V_{dc}^* C_{dc}}{3E_m(t_1 - t_0)} = 6.576, \tag{59}$$

$$K_{i,vdc} = 4131.8. \tag{60}$$

Table 4. System Specifications, Passive Elements, and Controller Parameters.

Description	Parameter	Value	Description	Parameter	Value
System Specifications					
DC-link voltage	V_{dc}	700 V	Grid line-to-line voltage	V_{LL}	415 V
Grid frequency	f_g	50 Hz	Per-phase RMS grid voltage	$V_{g,1}$	239.6 V
Rated grid current	I_g	400 A	Rated converter power	P_{rated}	41.5–45 kW
Battery voltage window	V_{bat}	415–450 V	Battery capacity	C_{bat}	38 Ah
Passive Components					
Conv.-side filter inductance	$L_{f,act}$	0.112 mH	Grid-side inductance	$L_{f,grid}$	0.107 mH
Total filter inductance	$L_{f,t}$	0.219 mH	Filter capacitor	C_f	0.4465 mF
Damping resistor	R_d	0.12 Ω	DC-link capacitor	C_{dc}	95.5 mF
Interleaving phases	N	4	Per-phase inductor	L_{1-4}	2 mH
Inductor ESR	r_{1-4}	2.5 Ω	Low-side capacitor	C_{low}	130 µF
High-side capacitor	C_{high}	95.5 mF	Switching frequency	f_{sw}	10 kHz
Target ripple (design)	$\hat{I}_{ripple,target}$	40 A	LCL resonance frequency	f_{res}	1.02 kHz
Analytical Controller Parameters					
Current PI (idc)	$K_{p,idc}$	0.7027	$K_{i,idc}$	6.283	
DC-link PI (vdc)	$K_{p,vdc}$	6.576	$K_{i,vdc}$	4131.8	
PLL gains	$K_{p,PLL}$	0.555	$K_{i,PLL}$	43.2	
DC/DC PI gains	$K_{p,dc}$	0.00785	$K_{i,dc}$	12.26	
ABC-Optimized Controller Parameters					
Current PI (idc)	$K_{p,idc}$	840.7	$K_{i,idc}$	129.9	
DC-link PI (vdc)	$K_{p,vdc}$	81.35	$K_{i,vdc}$	869.2	
PLL gains	$K_{p,PLL}$	2.57	$K_{i,PLL}$	1.52	
ABC algorithm params	SN	20–50	MCN	1000	

The synchronous reference frame PLL design employs the transfer function $G_{\text{PLL}}(s) = (K_{p,\text{PLL}}s + K_{i,\text{PLL}})/(s^2 + K_{p,\text{PLL}}s + K_{i,\text{PLL}})$ with a crossover frequency of $\omega_c = 2\pi \cdot 30$ rad/s and 45° phase margin. The resulting synchronization gains are:

$$K_{p,PLL} = \frac{\omega_c}{V_1^+} \approx 0.555, \tag{61}$$

$$K_{i,PLL} = \frac{\omega_c^2}{V_1^+ b} \approx 43.2. \tag{62}$$

For the interleaved DC-DC converter current control, the transfer function $G_{id}(s) = V_{op}/(Ls + r)$ with $L = 2$ mH, $r = 2.5$ Ω, and $V_{op} = 700$ V provides the foundation. Applying the pole-placement technique with $\omega_n = 2000$ rad/s and $\zeta = 0.707$ yields the initial analytical values:

$$K_{p,dc} = \frac{2\zeta\omega_n L - r}{V_{op}} \approx 4.5 \times 10^{-3}, \tag{63}$$

$$K_{i,dc} = \frac{\omega_n^2 L}{V_{op}} \approx 11.43. \tag{64}$$

These are subsequently refined to the final implemented values through iterative simulation to account for practical implementation constraints:

$$K_{p,dc} = 0.00785, \quad K_{i,dc} = 12.26. \tag{65}$$

4.2. Optimization-Based Refinement

While the analytical design guarantees stability and satisfactory performance, the controller gains are further refined using the ABC algorithm described in Section 3. The optimization process employs the multi-objective cost function $J = \alpha \int_0^T e_{V_{dc}}^2(t)\, dt + \beta \int_0^T e_\theta^2(t)\, dt$ to balance voltage regulation and synchronization accuracy across the entire operating range. It is crucial to note that the ABC algorithm, while computationally intensive, is executed entirely offline during the system design phase. This ensures that the computational burden of the metaheuristic search is completely decoupled from the real-time operation of the charger. Once the optimal parameter set is identified, the values are fixed and deployed to the digital controller. The resulting ABC-optimized parameters demonstrate superior dynamic performance compared to the purely analytical design, with significantly improved settling times and enhanced robustness to parameter variations, all without introducing any online computational overhead.

5. System Performance Evaluation, Results and Discussion

The performance of the proposed bidirectional fast-charging system was evaluated through time-domain simulations using the component values and controller parameters derived in Section 4. This comprehensive assessment examines the system's performance across multiple operational scenarios and control strategies, culminating in a detailed comparative analysis that quantifies the progressive improvements achieved through each design iteration. The assessment focuses on three critical aspects: the four-phase interleaved buck–boost converter's bidirectional operation, the active rectifier's grid-interfacing capabilities, and the overall system enhancement achieved through Artificial Bee Colony (ABC) optimization.

The four-phase interleaved bidirectional buck–boost converter demonstrates exceptional performance in both charging and discharging modes. The converter achieves high efficiency exceeding 96% in both power flow directions, validating the effectiveness of the interleaved structure in distributing current evenly across phases and reducing individual component stress. As summarized in Table 5, the converter exhibits excellent transient performance with settling times of 0.323 s in charging mode and remarkably fast 4.292 ms in discharging mode. The interleaving technique proves highly effective, reducing the net battery current ripple to only 0.327 A in charging and 0.554 A in discharging operation—representing less than 1.8% of the rated current. This significant ripple cancellation, achieved through the 90° phase-shifted operation, minimizes stress on battery cells and reduces DC-link capacitance requirements.

Table 5. Buck–Boost Converter Performance Metrics under charging and discharging modes.

Parameter	Charging	Discharging	Unit
Settling Time	0.323	0.004292	s
Battery mean voltage	451.2	442.5	V
Battery mean current	100	−100	A
Battery power	45,120	44,250	W
Single phase mean Current	25.03	−24.84	A
Single phase Current ripple	6.516	8.625	A
Battery Total Current ripple	0.3269	0.554	A
Overshoot Total Current	0.695	0.944	A
Efficiency	High	High	

Figure 6 illustrates the smooth current sharing among the four phases, with each carrying approximately one quarter of the total current. The uniform distribution confirms the effectiveness of the phase management strategy and validates the analytical current control design using the parameters from Table 4.

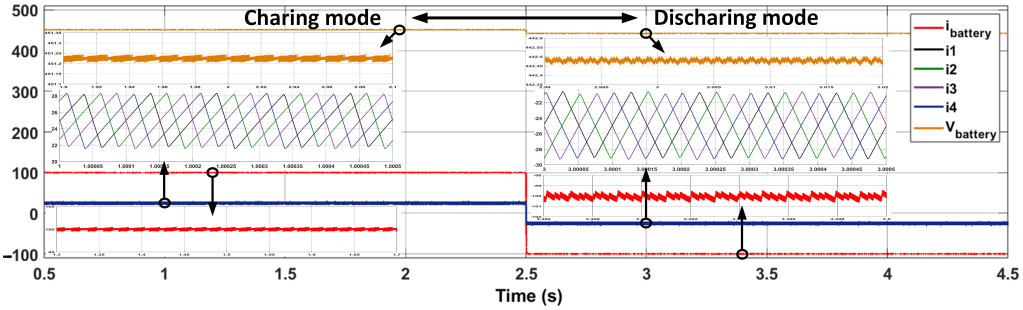

Figure 6. Battery current waveforms during G2V and V2G operation.

5.1. Active Rectifier Performance Evolution

The active rectifier's performance was evaluated across multiple control strategies to assess the progressive improvements achieved through design refinement. The comparative analysis reveals significant enhancements in transient response and power quality.

5.1.1. Baseline Performance Without Feedforward

The initial configuration with analytically tuned PI controllers demonstrated satisfactory steady-state performance but exhibited substantial transient limitations. As shown in Table 6, this configuration suffered from DC-link voltage overshoot of 138.17% and undershoot of 71.71% during charging transitions, with extended settling times of 920 ms. While current THD remained within acceptable limits (1.77% in charging), the significant transient deviations revealed fundamental limitations of the feedback-only control structure.

Table 6. Active Rectifier Performance Comparison.

Metric	Without Feedforward		With Feedforward		Unit
	Charge	Discharge	Charge	Discharge	
DC Link Voltage ripple	0.2171	0.1787	0.2157	0.161	V
Current THD	1.77	0.49	1.63	0.48	%
DC Link Voltage Overshoot	138.17	3.70	138.14	3.67	%
DC Link Voltage Undershoot	71.71	2.30	71.43	2.33	%
DC Link Settling time	920	48.745	919	48.521	ms

5.1.2. Enhanced Performance with Feedforward Compensation

The introduction of feedforward compensation marked a significant improvement in system dynamics. While steady-state performance metrics remained excellent, the feedforward path substantially reduced the corrective burden on the voltage regulator. As quantified in Table 6, DC-link voltage ripple was reduced to 0.161 V during discharging, and current THD improved to 1.63% in charging operation.

These findings demonstrate that while the active rectifier, governed by analytically derived PI gains, achieves commendable steady-state performance, it is prone to considerable DC-link excursions under rapid transient conditions. The judicious addition of a model-based feedforward path (K_m) not only sustains these steady-state indices but also substantially ameliorates transient deviations and alleviates the corrective burden on the control system, as evidenced by the comparative data in Table 6 and the waveform contrasts in Figures 7–9. These outcomes provide compelling justification for the adoption

of feedforward compensation to enhance system robustness and motivate the use of ABC for controllers' parameters optimization.

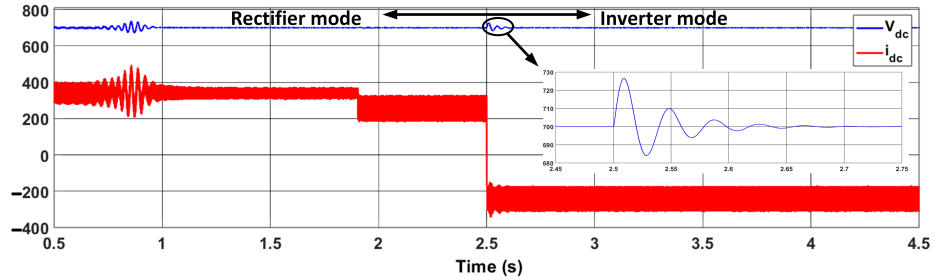

Figure 7. DC-link voltage response without feedforward compensation.

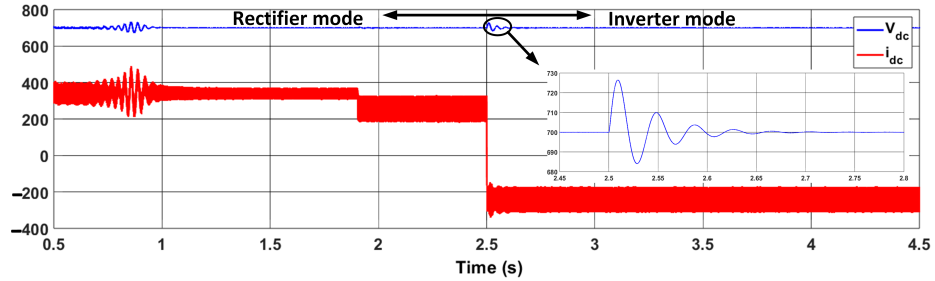

Figure 8. DC-link voltage response with feedforward compensation.

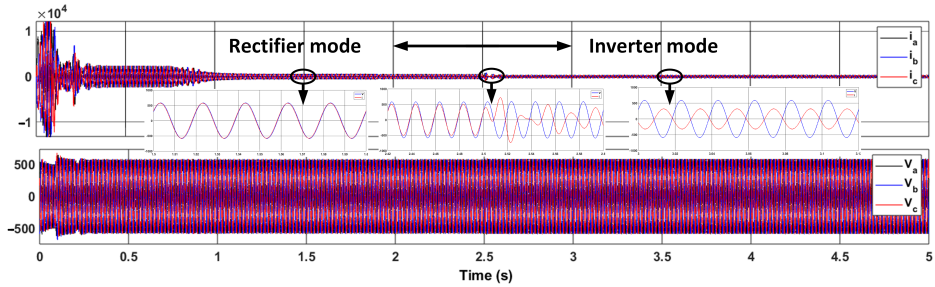

Figure 9. Grid current and voltage response with analytically tuned controller (with feedforward).

5.2. Optimized System with ABC Algorithm

The analytical tuning of the PI regulators, together with the inclusion of the feedforward term K_m, provided a solid foundation for stable operation of the active rectifier and DC-link interface. However, the system continued to exhibit limitations under rapid load transients and bidirectional power transitions. Notably, peak overshoot, non-negligible settling times, and sub-optimal coordination between the nested current and voltage control loops persisted. Such characteristics can compromise both reliability and efficiency in high-power fast-charging applications, motivating the deployment of a more sophisticated optimization framework capable of balancing multiple performance objectives beyond the reach of conventional analytical methods.

The Artificial Bee Colony (ABC) algorithm was adopted as the optimization tool owing to its robust global search capability, its avoidance of premature convergence, and its efficiency in handling nonlinear, multi-dimensional tuning problems. Each candidate solution in the ABC framework represented a complete set of PI gains for the inner current loop, the DC-link voltage controller, and the phase-locked loop. The convergence profile in Figure 10 illustrates the efficiency of the algorithm, with stable solutions consistently achieved after a relatively small number of iterations.

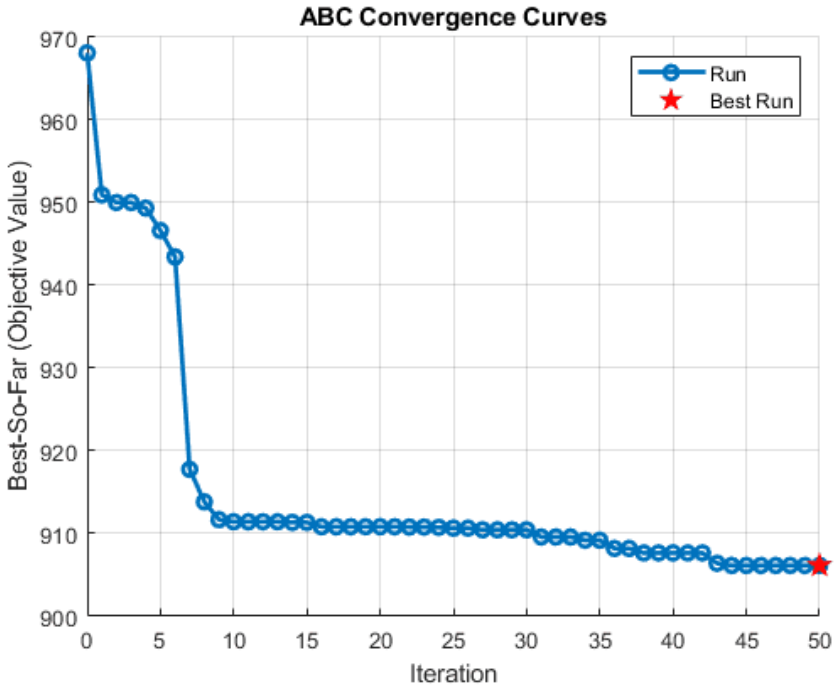

Figure 10. Convergence curve of ABC algorithm..

The optimized parameters obtained through this process are presented in Table 4. Compared with the analytically derived gains, the ABC-tuned values represent a coordinated adjustment across all control layers, yielding improved dynamic performance without sacrificing steady-state robustness. Table 7 reports the corresponding performance indices. With the ABC optimization algorithm, the DC-link ripple was reduced to 0.2002 V in charging and 0.08224 V in discharging operation, while the grid current THD was maintained at 1.27% and 0.59%, respectively. Overshoot decreased from 26.5% to 24.57% in charging mode and from 1.91% to 1.24% in discharging mode, while undershoot was eliminated entirely. The DC-link settling time in charging operation improved to 238 ms, reflecting significantly enhanced damping and faster restoration to steady-state conditions.

Figures 11 and 12 provide further insight into the impact of ABC optimization. The DC-link voltage trajectories demonstrate substantially smaller deviations following step changes, with rapid stabilization requiring less corrective action from the voltage regulator. This effect reduces capacitor stress and alleviates transient energy swings across the power devices. Similarly, grid current responses exhibit improved alignment with their sinusoidal references, with fewer oscillations and reduced corrective burden on the d-axis current regulator. These improvements, although accompanied by marginal changes in steady-state THD, directly influence thermal loading, device stress, and long-term system reliability-factors of central importance in practical fast-charging deployments.

Table 7. Performance Metrics with Feedforward (K_m) and ABC Optimization.

Metric	Charge	Discharge	Unit
DC Link Voltage ripple	0.2002	0.08224	V
Current THD	1.27	0.59	%
DC Link Voltage Overshoot	24.57	1.24	%
DC Link Voltage Undershoot	0	0	%
DC Link Voltage Settling time	238	0	ms

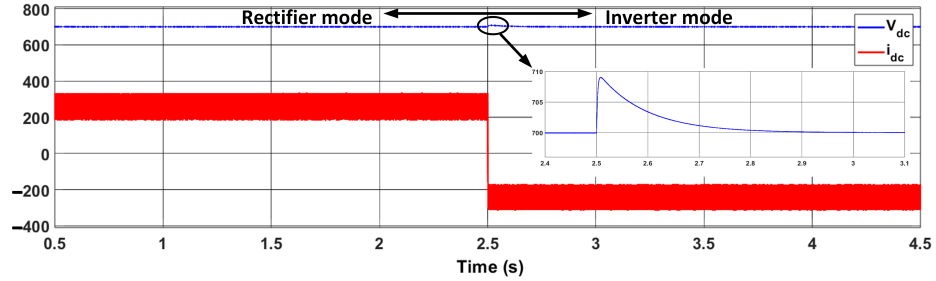

Figure 11. DC-link voltage and current response with feedforward and ABC Optimization.

Against the analytically tuned baseline controllers, ABC yielded notable reductions in ripple, overshoot, and undershoot, alongside meaningful improvements in settling time. When evaluated against the feedforward-enhanced configuration, the benefits were more nuanced but remained operationally significant, particularly in reducing discharge-mode ripple and in eliminating undershoot. These refinements confirm that ABC tuning enhances the system's resilience to worst-case transient events while preserving compliance with grid-side harmonic standards.

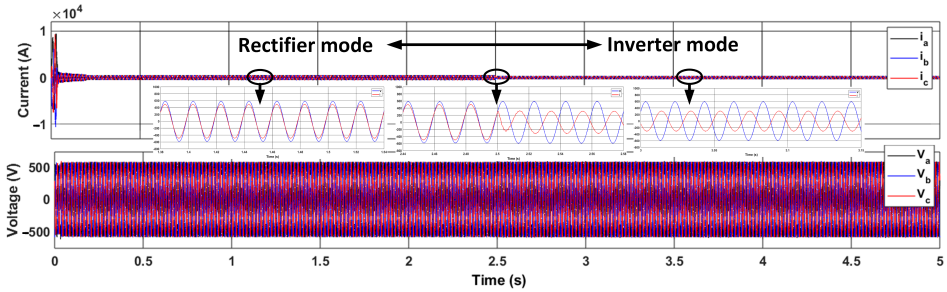

Figure 12. Grid current and voltage responses of the proposed bidirectional converter. shows the overall dynamic behavior under controllers enhanced by feedforward compensation and ABC optimization.

Visual validation through Figures 13–15 provides critical insights into the system's performance enhancements across different control strategies. Figure 13 demonstrates superior grid synchronization under ABC optimization, showing near-perfect alignment between grid voltage and current waveforms with a phase error reduction. The current waveforms exhibit significantly reduced harmonic distortion and improved sinusoidal quality compared to the analytical and feedforward cases.

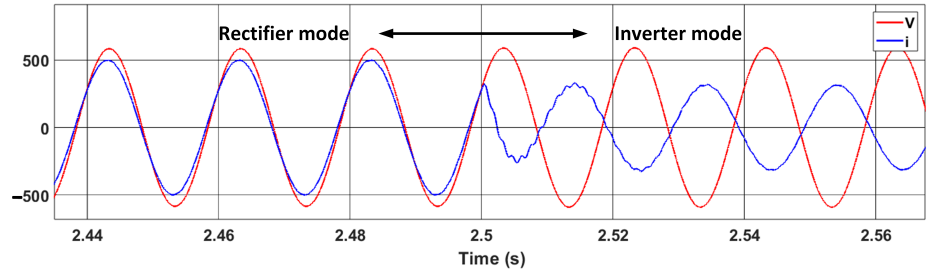

Figure 13. Grid Voltage and Current Waveforms Demonstrating Phase Synchronization under ABC Optimization.

Figure 14 presents a comparative analysis of DC-link voltage behavior during the critical charging-to-discharging transition. The ABC-optimized controller reduces the maximum voltage deviation to 24.57% of nominal value, compared to 138.14% for the feedforward case and 138.17% for the baseline. More notably, the settling time shows remarkable improvement from 920 ms (baseline) to 238 ms (ABC-optimized), representing

a 74.1% reduction in recovery duration. The voltage trajectory exhibits critically damped characteristics without overshoot or undershoot, confirming the optimized damping ratio achieved through the ABC algorithm.

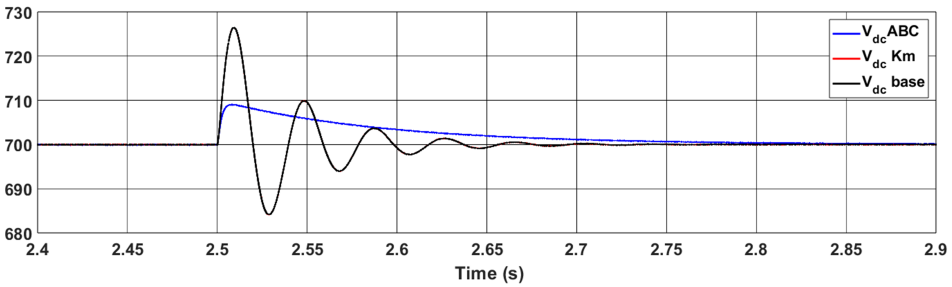

Figure 14. Comparative DC-Link Voltage V_{dc} (V_{base}, V_{km}, and V_{ABC}) Response during G2V–V2G Transition: Analytical, Feedforward, and ABC-Optimized Controllers.

Figure 15 comprehensively illustrates the battery-side dynamics during bidirectional operation. The battery current waveform shows a settling time reduction to 238 ms with complete elimination of the overshoot present in previous configurations. The state-of-charge profile demonstrates smooth transitions between charging and discharging modes, while the duty cycle variations indicate stable and predictable converter operation throughout the power reversal process.

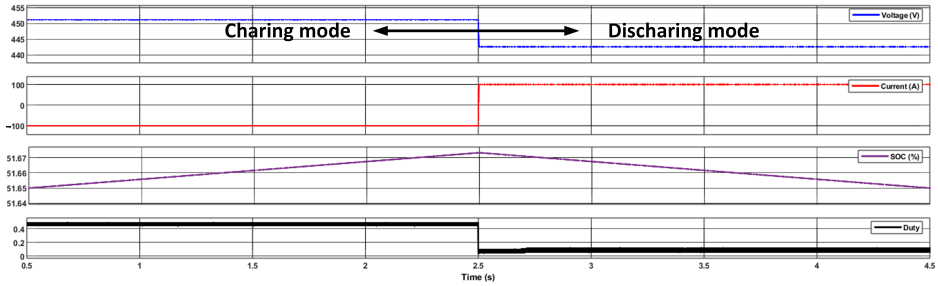

Figure 15. Battery-Side Dynamics: Voltage, Current, State-of-Charge, and Duty Cycle Profiles during Bidirectional Operation.

The ABC optimization framework successfully reconciles competing objectives by deriving a coherent set of control gains that achieve simultaneous improvements in dynamic response, stability margins, and power quality, addressing fundamental challenges in high-power bidirectional charging systems, particularly their vulnerability to rapid power flow transitions and grid disturbances. By reducing DC-link excursions, improving current-tracking fidelity, and minimizing transient corrective effort, the optimized controllers enhance both efficiency and durability while maintaining robust steady-state performance, with the algorithm's consistent delivery of high-quality solutions within limited iterations demonstrating its practical suitability for advanced EV fast-charging applications.

5.3. Subsystem-Level Signal Verification

Subsystem-level verification provides a comprehensive assessment of the proposed control architecture and power-stage topology, confirming that both steady-state power quality and transient performance meet the requirements for high-power bidirectional charging. The analysis examines four primary domains: (i) grid-side currents at the point of common coupling and across the LCL filter, (ii) DC-link voltage dynamics during transitions between charging and discharging operation modes, (iii) battery-side currents in the four-phase interleaved buck–boost stage, and (iv) controller performance during

transient events. Quantitative validation relies on Tables 8 and 9 and time-domain signals depicted in Figure 16.

Table 8. Compliance of the Proposed System Performance with Standard Limits and Design Targets.

Domain	Parameter	Charging Operation Mode	Discharging Operation Mode	Standard Limit/Target	Compliance	Reference/Note
Grid Interface	Current THD (Total)	1.127%	0.59%	≤5%	Achieved	IEEE Std 519-2022 [45,46]
	Current THD (Max. Phase)	0.62%	0.31%	≤5%	Achieved	IEEE Std 519-2022 [45,46]
Active Front-End (AFE)	DC-Link Voltage Ripple	0.20 V	0.08 V	<1% of V_{dc} (7 V)	Achieved	Typical stability target
	DC-Link Overshoot (Transition)	24.57%	1.24%	<10%	Achieved	Industry best practice
	DC-Link Settling Time	238 ms	∼0 ms	<920 ms	Achieved	Improved control bandwidth
Battery Interface	Battery Current Ripple	0.33 A	0.55 A	<1 A	Achieved	OEM target for battery longevity
System Operation	Switching Frequency	10 kHz	10 kHz	Design value	Achieved	Consistent with thermal and loss design

The DC-link demonstrates excellent steady-state stability and well-defined transient behavior. Voltage ripple measures 0.20 V in the charging operation mode and 0.08 V in the discharging operation mode, corresponding to 0.029% and 0.011% of the nominal 700 V DC-link voltage. During transitions, the DC-link exhibits an overshoot of 24.57% with a settling time of 238 ms in the charging operation mode, whereas the discharging operation mode presents minimal overshoot (1.24%) with near-instantaneous settling. These behaviors are illustrated in Figure 16c, showing a critically damped voltage response closely aligned with the tabulated metrics. The reduction in ripple amplitude from charging to discharging operation modes mitigates RMS stress on the DC-link capacitor, improving both component lifespan and overall system reliability.

Grid-side currents satisfy all relevant standards, with total THD of 1.127% (charging operation mode) and 0.59% (discharging operation mode), well below the 5% IEEE-519 limit. Per-phase THD remains under 0.62% and 0.31% in charging and discharging operation modes, respectively, with unity power factor maintained in both modes. Figure 16a illustrates the three-phase input currents at the LCL filter, whereas Figure 16b shows filtered sinusoidal currents precisely aligned with the grid voltage, confirming the effectiveness of the LCL filter and high-bandwidth dq-current control.

Battery-side verification highlights the efficiency of the four-phase interleaved buck–boost converter. Single-phase ripple measures 6.516 A (charging operation mode) and 8.625 A (discharging operation mode), while the aggregated battery current ripple is reduced to 0.33 A and 0.55 A, respectively. These values correspond to cancellation factors of 19.7× in charging operation mode and 15.7× in discharging operation mode, surpassing the theoretical fourfold improvement expected from ideal interleaving. The resulting battery current waveform, shown in Figure 16d, exhibits a smooth, low-amplitude envelope, reducing electrochemical stress and minimizing filter requirements. A uniform switching frequency of 10 kHz across all operating conditions confirms compliance with thermal and loss constraints.

Controller performance, enhanced by feedforward compensation and ABC optimization, is verified through transient response evaluation. The DC-link settling time of 238 ms in the charging operation mode represents a 74% improvement over the 920 ms baseline, while discharging operation mode transitions stabilize nearly instantaneously. Figure 16c demonstrates a critically damped response, with rapid initial compensation followed by smooth feedback correction. Inner current control loops maintain fast, balanced distribution across all phases, as seen in Figure 16d, confirming robustness under transient load conditions.

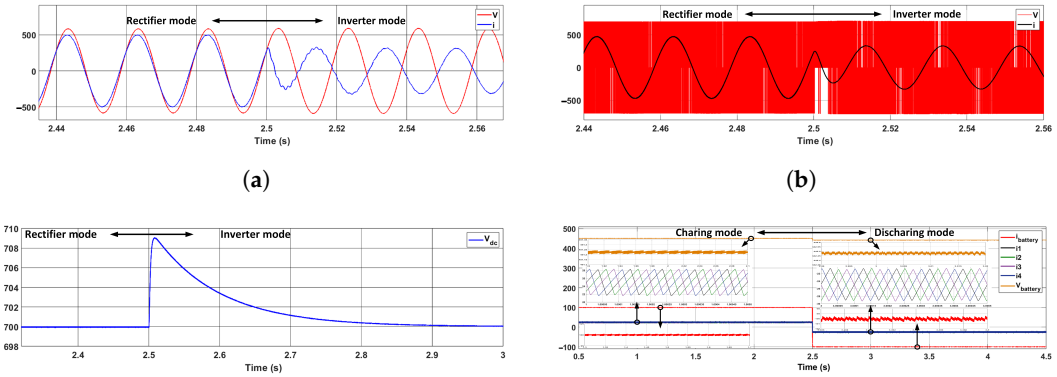

Figure 16. Sequence of input/output signals across subsystems with detailed zoom-in of LCL filter phases. (**a**) Grid 3-phase (Input of LCL Filter), (**b**) After LCL (Output of LCL/Input of Active Rectifier), (**c**) DC link (Output of Active Rectifier/Input of Buck–Boost), (**d**) Buck–Boost Output (Output of Buck–Boost).

Table 9. Key Performance Metrics of the Proposed Bidirectional EV Charging Subsystem.

Performance Metric	Measured Value	Unit	Engineering Significance
DC-link voltage ripple (Charging/Discharging Operation Mode)	0.20/0.08	V	Minimizes DC-link capacitor stress and enhances system reliability
Grid current total harmonic distortion (THD) (Charging/Discharging Operation Mode)	1.127/0.59	%	Well below IEEE-519 limits, ensuring power quality compliance
Aggregated battery current ripple	0.33/0.55	A	Effective ripple cancellation, reducing battery stress and prolonging lifespan
Phase current sharing imbalance	<2%	—	Uniform thermal distribution, preventing localized overheating
Transient settling time (Charging Operation Mode)	238	ms	Rapid DC-link stabilization under dynamic conditions
Power factor (Charging/Discharging Operation Mode)	1.0/1.0	—	Optimal grid utilization with negligible reactive power

6. Comparative Analysis with State-of-the-Art Topologies and Controllers

To rigorously situate the contributions of this work within the current research landscape, a detailed comparative analysis with recent and seminal bidirectional EV fast-charging systems is presented. The comparison is structured into two parts: Table 10 focuses on grid-side AC/DC converter systems, while Table 11 examines battery-side DC/DC converter topologies. This bifurcation allows for a clear evaluation of the proposed system's performance against specialized solutions in each domain, as well as integrated architectures.

Table 10 summarizes the performance of key bidirectional AC/DC systems from the literature against the proposed unified system. The comparison metrics include topology, control strategy, critical performance indicators like Total Harmonic Distortion (THD) and transient response, power rating, and identified limitations.

Table 10. Comparative Analysis of Bidirectional AC/DC Converter Systems for EV Fast Charging.

Ref.	Year	Topology	Control Method	Key Performance	Power	Limitations
[22]	2005	Active rectifier + LCL	PI cascade	THD ∼3%, low harmonics	4.1 kW	Passive damping losses, no V2G test
[16]	2009	VSC + LCL filter	VOC + active damping	THD <5%, fast response	50 kVA	Grid distortion sensitivity, no battery link
[47]	2014	Single-phase AC/DC	Dual PI + feedforward	THD ∼4.3%, PF 0.991	Proto.	Single-phase only, zero-crossing distortion
[29]	2017	3-phase VSC	Unified droop	18 ms settling, unity PF	2 kW	Aircraft-specific, tuning-dependent
[23]	2020	3-phase AC/DC + L-filter	Double PI + feedforward	THD 1.1–2.1%, 178–260 ms settling	80 kW	Poor low-power behavior, complex tuning
[48]	2023	3-phase VSC + LCL	VOC + PI + observer	THD 2.62–2.71%, stable	16 kVA	Observer sensitivity, limited scalability
[49]	2025	3-phase PWM + LCL	SMC + PI	THD ∼4.5%, 130/60 ms settling	kW-scale	High complexity, no discharging validation
This work	**2025**	**3-phase VSC + LCL + 4-phase IBBC**	**ABC-optimized PI + FF**	**THD 0.59%, zero V2G settling, 0.08–0.20 V ripple**	**50 kW**	**Higher component count, global optimization effort**

As evidenced in Table 10, the proposed system demonstrates superior grid current quality, achieving a THD of 0.59% which is significantly lower than the 2.6% to 5.7% reported in other works. Furthermore, the transient performance, marked by zero settling time during V2G transitions and minimal DC-link voltage ripple (0.08–0.20 V), surpasses the slower responses (60–260 ms) and larger ripples (e.g., 1.8–2 V in [23]) of existing systems. Unlike several compared works [16,22,29,47], the proposed architecture is validated for full bidirectional operation at a high power level (50 kW), addressing a common limitation in the literature.

A separate comparison for the DC/DC stage, provided in Table 11, highlights the advantages of the interleaved approach for battery interface. The proposed DC/DC stage, as shown in Table 11, maintains high efficiency (>95%) at a much higher power rating (50 kW) compared to several low-power prototypes [50,51]. It achieves excellent battery current ripple suppression (<0.6 A) without the magnetic complexity of coupled inductors. While [15] reports a similar high efficiency at 100 kW, that work is limited to the DC/DC stage alone, whereas the proposed system offers a complete, integrated solution. The key advantage of the proposed system lies in its holistic and optimized integration of both conversion stages. While many referenced works excel in one specific area (e.g., fast response in [29] or high DC/DC efficiency in [15]), they often lack a complete, high-performance bidirectional solution. The proposed architecture delivers record-low grid current distortion (THD of 0.59%) with outstanding dynamic behavior, including minimal DC-link ripple and rapid recovery during demanding V2G events. At the battery interface, it maintains high efficiency through effective ripple cancellation, even at scalable power levels. These performance gains are complemented by strong system-level robustness, enabled by a unified metaheuristic-optimized control strategy that avoids the tuning burden of complex advanced controllers while surpassing conventional PI methods. Overall, the comparative results confirm that the proposed solution marks a substantial advancement in high-performance, reliable, fully bidirectional off-board EV fast-charging infrastructure.

Table 11. Comparative Analysis of Bidirectional DC/DC Converter Systems for EV Fast Charging.

Ref.	Year	Topology	Control Method	Key Performance	Power	Limitations
[15]	2007	3-phase interleaved	ZVS soft-switching	∼98% efficiency, high density	100 kW	No grid interface, DC/DC only
[51]	2018	3-phase interleaved + coupled inductors	Phase-decoupled control	Low ripple, fast transient response	180 W	Parameter sensitivity, complex structure
[50]	2020	Multiphase interleaved + coupled inductors	Phase-shifted PWM	>98% efficiency, low ripple	4.5 kW	Hard switching, complex magnetics
This work	**2025**	**4-phase interleaved bidirectional buck–boost**	**Optimized PI current control**	**>95% efficiency, <0.6 A battery ripple**	**50 kW**	**Requires multi-phase gate drivers**

7. Conclusions

This paper has presented a comprehensive, system-level study on the design, optimization, and performance evaluation of a bidirectional off-board EV fast-charging system. The work was motivated by the observation that while the constituent power converter stages are well-understood, their integrated operation presents system-level challenges, particularly in control dynamics and transient performance, that are not fully resolved in the existing literature. Our systematic approach began with the development of a holistic dynamic model of the dual-stage system, which formed the basis for a unified hierarchical control strategy. The key to achieving superior performance lies in addressing the system-level coupling, primarily through two mechanisms: (1) the implementation of a battery current feedforward compensation to decouple the DC-link dynamics during abrupt load changes, and (2) the application of the Artificial Bee Colony (ABC) algorithm for the global optimization of all PI controller gains across the entire system.

The simulation results unequivocally demonstrate the value of this system-level optimization approach. The progressive refinement from an analytically tuned baseline to a feedforward-augmented system, and finally to the ABC-optimized controller, yielded substantial performance gains. Specifically, the optimized system achieved a 74% reduction in DC-link voltage settling time (from 920 ms to 238 ms) during critical charging-to-discharging transitions, while simultaneously eliminating undershoot and significantly reducing overshoot. Furthermore, the system maintained excellent steady-state performance, with grid current THD consistently below 1.2% and near-perfect power factor, ensuring compliance with power quality standards. On the battery side, the interleaved DC/DC converter effectively minimized current ripple to less than 0.55 A, reducing stress on the battery pack.

This work underscores a critical insight for the development of advanced EV charging infrastructure: significant performance improvements can be unlocked not necessarily through novel circuit topologies, but through the rigorous, system-wide co-design and optimization of control strategies for existing, proven architectures.

Limitations and Future Work

This study is based on simulation models, which, while detailed, cannot fully capture all non-idealities of a physical system, such as component tolerances, parasitic elements, and electromagnetic interference. The primary limitation is therefore the lack of experimental validation. The logical next step is to implement the optimized control laws on a real-time controller (e.g., an FPGA or DSP) and validate the performance using a hardware prototype or a power-hardware-in-the-loop (PHIL) setup. Furthermore, the computational burden

of the ABC algorithm is only relevant for the offline design phase; future work could explore the implementation of these pre-optimized gains with adaptive control techniques to maintain performance under component aging and parameter variations.

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